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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,343	09/19/2003	Sailesh Kottapalli	42P17404	8176

8791 7590 11/15/2006

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,343	KOTTAPALLI, SAILESH	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-29 have been considered. Claims 1-29 have been amended as per Applicants' request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 24 August 2006.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-12, and 14-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sprangle and Patt's "Facilitating Superscalar Processing via a Combined Static/Dynamic Register Renaming Scheme" ©1994 (herein referred to as Sprangle) in view of Arora et al., U.S. Patent Number 5,832,260 (herein referred to as Arora).

5. Referring to claims 1, 10, 18, and 24, taking claim 24 as exemplary, Sprangle has taught a system, comprising:

a. A processor, including

i. A decode circuit to decode an original instruction into a predicate-positive instruction and a predicate-negative instruction (Sprangle Section 6; Table 4; Table 5; and Table 6);

ii. A register renaming circuit to map a first destination register of the predicate-positive instruction to a physical register, and to map a second destination register of the predicate-negative move instruction to the same physical register (Sprangle Section 6; Table 4; Table 5; and Table 6); and

iii. A retirement circuit to update said physical register with a result of either the predicate-positive instruction or the predicate-negative move instruction responsive to a predicate value associated with both instructions (Sprangle Section 6; Table 4; Table 5; and Table 6). In regards to Sprangle, the second or move instruction is executed based upon a predicate value and the result is used in the multiply instruction, so the results of the second or move instruction had to have been retired for the multiply to execute correctly.

b. A bus to couple the processor to input/output devices (Arora column 5, lines 20-23 and Figure 2); and

c. A communications device coupled to the bus (Arora column 4, lines 63-66 and Figure 2).

6. Sprangle has not taught the predicate-negative instruction is a move instructions. Arora has taught that any instruction can be part of a predicate instruction sequence, including move instructions (Arora column 3, lines 21-54 and Figure 1). A person of ordinary skill in the art at the time the invention was made, and as taught by Arora, would have recognized that the predicate instructions of Arora removes the misprediction penalty associated with short branches (Arora column 3, lines 46-47), thereby improving throughput and performance of the

microprocessor (Arora column 2, lines 49-58). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the predicate instructions of Arora in the device of Sprangle to improve throughput and performance.

7. Claims 1, 10, and 18 are substantially similar to claim 24 and rejected for the same reasons. The only difference is that claims 10 and 18 are for a processor and claim 1 is a method while claim 24 is a system.

8. Referring to claims 2, 11, 19, and 25, taking claim 25 as exemplary, Sprangle in view of Arora has taught wherein the predicate-negative move instruction is responsive to a complement of the predicate value (Sprangle Section 6; Table 4; Table 5; and Table 6).

9. Referring to claims 3, 12, 20, and 26, taking claim 26 as exemplary, Sprangle in view of Arora wherein the decode circuit sends a hint to the register renaming circuit to permit the mapping of the first destination register and the second destination register to the same physical register. (Sprangle Section 6; Table 4; Table 5; and Table 6). In regards to Sprangle, the two resulting instructions write to the same tag and the renaming tag is maintained for dependent instructions, as show in Tables 5 and 6 with the DIV, ADD, and MULT instructions, so there must be some identification, i.e. hint, showing the dependency when it is sent to the renaming circuit.

10. Referring to claims 5, 14, 21, and 27, taking claim 27 as exemplary, Sprangle in view of Arora has taught a sequencer to permit out-of-order execution of the predicate-positive instruction and the predicate-negative move instruction (Arora column 1, lines 25-31).

11. Referring to claims 6, 15, 22, and 28, taking claim 28 as exemplary, Sprangle in view of Arora has taught, wherein the retirement circuit squashes the predicate-negative move instruction

when the predicate-positive instruction executes before the predicate-negative move instruction and the predicate value is true (Sprangle Section 6; Table 4; Table 5; and Table 6).

12. Referring to claim 7, Sprangle in view of Arora has taught wherein the squashing occurs before the predicate-negative move instruction executes (Sprangle Section 6; Table 4; Table 5; and Table 6).

13. Referring to claims 8, 16, 23, and 29, taking claim 29 as exemplary, Sprangle in view of Arora has taught wherein the retirement circuit squashes the predicate-negative instruction when the predicate-negative move instruction executes before the predicate-positive instruction and the predicate value is false (Sprangle Section 6; Table 4; Table 5; and Table 6).

14. Referring to claim 9, Sprangle in view of Arora has taught wherein the squashing occurs before the predicate-positive instruction executes (Sprangle Section 6; Table 4; Table 5; and Table 6).

15. Referring to claim 17, Sprangle in view of Arora has taught execution units to execute the predicate-positive instruction and the predicate-negative move instruction in parallel (Sprangle Section 1).

16. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sprangle and Patt's "Facilitating Superscalar Processing via a Combined Static/Dynamic Register Renaming Scheme" ©1994 (herein referred to as Sprangle) in view of Arora et al., U.S. Patent Number 5,832,260 (herein referred to as Arora), as applied to claim 3 above, and further in view of Rodgers et al., U.S. Patent Number 6,496,925 (herein referred to as Rodgers). Taking claim 4 as exemplary, Sprangle in view of Arora has not taught wherein the sending includes sending the hint via a trace cache. However, Sprangle has taught the two resulting instructions write to the

same tag and the renaming tag is maintained for dependent instructions, as show in Tables 5 and 6 with the DIV, ADD, and MULT instructions. Rodgers has taught that trace caches contains pointers for preceding and proceeding instructions, e.g. showing dependencies among instructions (Rodgers column 7, lines 20-62). A person of ordinary skill in the art at the time the invention was made, and as taught by Rodgers, would have recognized that trace caches increases instruction bandwidth (Rodgers column 7, lines 31-32) and facilitates high-performance instruction sequencing (Rodgers column 7, lines 38-42). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the trace cache of Rodgers in the device of Sprangle in view of Arora to increase instruction bandwidth and facilitate high-performance instruction sequencing.

Response to Arguments

17. Applicant's arguments filed 24 August 2006 have been fully considered but they are not persuasive. Applicant's argue in essence on pages 8-11

> Applicant submits that Sprangle does not disclose or suggest decoding an original instructions into a complementary-predicated pair of instructions including a predicate-positive instruction and a predicate-negative move instructions...

18. This has not been found persuasive. Sprangle has disclosed on pages 145-146, section 6 Predicated Execution & Register Renaming, and as illustrated in Sprangle's Table 4, the high language branch program instruction is decoded into multiple predicate instructions. The predicate instructions include a predicate-positive, i.e. what to do when the predicate is true, and a predicate-negative, i.e. what to do when the predicate is false, instructions. As shown in the above rejection, Arora was used to teach the specific move instruction.

Conclusion

19. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

20. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Karp et al., U.S. Patent Number 5,748,936, has taught a system with predicate instructions.

b. Hsu, U.S. Patent Number 5,901,318, has taught creating predicate instructions from branch instructions.

c. Santhanam, U.S. Patent Number 6,286,135, has taught a compiler creates predicate instructions from conditional branch instructions.

d. Gillies et al., U.S. Patent Number 6,834,383, has taught compiling conditional branches into predicate instructions and executing the predicate instructions.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

23. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

24. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
13 November 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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